

CLAIM REVISIONS

1 1. (AMENDED) A signal router, comprising:

2 a ~~signal transducer~~ conditioning circuit configured to write ~~J-K~~ identical
3 images of a first set of data from N inputs to ~~J-K~~ random access memories during a first
4 time interval;

5 ~~M-K~~ respective bit selectors each configured to read respective portions of
6 a respective one of said ~~J-K~~ identical images;

7 ~~each of said K~~ respective bit selectors being ~~further configured~~ coupled to
8 construct a ~~respective one of K-M~~ output data streams during a second time interval

9 wherein each of the random access memories comprises exactly two parts
10 configured so that during the second time interval a read occurs from a first one of the
11 parts, while a write occurs to a second one of the parts.

1 2. (canceled)

1 3. (amended) A signal router, as in claim 1, wherein said ~~signal~~

2 ~~transducer~~ conditioning circuit includes a buss to which said first set of data is

3 applied and addressing controllers configured to write data from said buss to said

4 random access memories, whereby said ~~J-K~~ identical images are written.

1 4. (AMENDED) A signal router, comprising:

2 a controller programmed to store identical images of data from said N
3 inputs in K memories;

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4 said controller being further programmed to read respective bits of said
5 data from each of said K memories to produce ~~K-M~~ respective output data streams,
6 whereby N inputs are mapped to ~~K-M~~ outputs,
7 wherein each of the K memories comprises exactly two parts configured
8 so that during the second time interval a read occurs from a first one of the parts, while a
9 write occurs to a second one of the parts.

1 5. A router as in claim 4, further comprising a data buss connected to receive said N
2 inputs and distribute them to said K memories.

1 6. A router as in claim 5, wherein a bit rate of each of said K outputs is less than a
2 bit rate of said buss.

1 7. (AMENDED) A method of routing data from N inputs to M outputs, comprising
2 the steps of:
3 applying data from said N inputs to a data buss by means of at least one of
4 time and space multiplexing;
5 imaging said data on ~~M-K~~ random access memories from said buss;
6 reading respective sets of bits from said random access memories to form
7 respective ones of said signals ultimately demultiplexed to form said M outputs,
8 wherein each of the random access memories comprises exactly two parts
9 configured so that during the second time interval a read occurs from a first one of the
10 parts, while a write occurs to a second one of the parts.

1 8. (new) The router of claim 1, wherein the parts are configured so that upon completion of the
2 second interval, the first and second parts change roles, so that subsequently the first part is used
3 for the write and the second part is used for the read.

1 9. (new) The router of claim 4, wherein the parts are configured so that upon completion of the
2 second interval, the first and second parts change roles, so that subsequently the first part is used
3 for the write and the second part is used for the read.

1 10. (new) The method of claim 7, wherein the parts are configured so that upon completion of
2 the second interval, the first and second parts change roles, so that subsequently the first part is
3 used for the write and the second part is used for the read.

1 11. (new) A signal router, comprising:

- 2 • N inputs for receiving synchronous streams of serial broadcast data;
- 3 • a conditioning circuit configured to write K identical images of a first set of data from the N
4 inputs to K during a first time interval;
- 5 • K respective bit selectors each configured to read respective portions of a respective one of
6 said K identical images; and
- 7 • each of said K respective bit selectors being coupled to construct M output data streams
8 during a second time interval.